A DOPPLER SONAR CONTROLLER

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Abstract

Accurate measurements of the upper ocean velocity field can now be made using Doppler sonar. Doppler measurements can be made with a wide variety of transducers provided that signal generation and echo processing techniques suitable for Doppler are applied. This paper describes a Doppler sonar controller which was designed to operate a variety of experimental Doppler systems. The controller can generate sequences of eight tones, each with independently prescribed frequency, duration and start time. The received echos are complex heterodyned and low-pass filtered to remove the carrier frequencies. The data is then passed to a computer for subsequent analysis. A simplified method of digital frequency synthesis used in the controller is described. The controller has proven to be exceptionally versatile in both oceanic and laboratory tests.

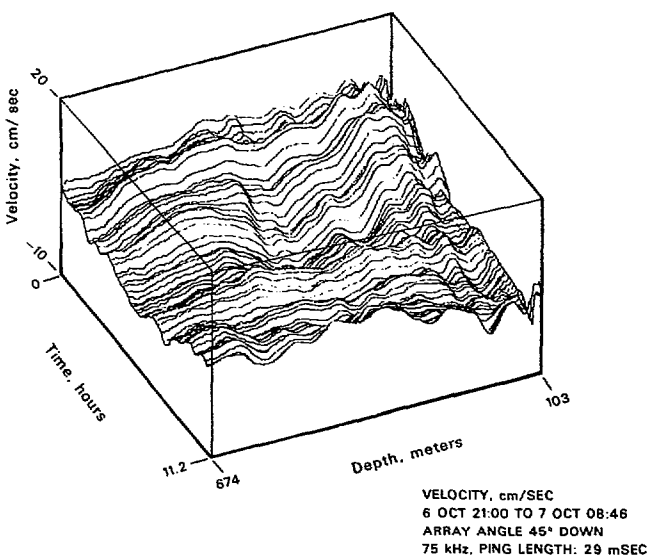

Figure 1. A deformed surface map of the along beam component of water velocity vs depth and time. Positive displacement of the surface represents toward FLIP velocity. The data were taken by a Doppler sonar mounted on the bottom of FLIP (depth) 87 m) and directed 45° downward.

Introduction

Doppler sonar is rapidly becoming a useful tool for the remote measurement of the upper ocean velocity field. In this approach, sound is transmitted in a narrow beam. The sound scatters off the plankton and nekton in the beam. From the Doppler shift of the returning echo the component of scatterer velocity parallel to the sonar beam can be determined at many ranges. Sonar velocity measurements have been made from the Research Platform FLIP out to a distance of 1.6 km, with 25 m range resolution. The information obtained from the single sonar is equivalent to that from a linear array of 64 one-component current meters. An example of a Doppler velocity map is presented in Figure 1.

Doppler measurements can be made with a wide variety of transducers, provided that the processing of the received signal is properly synchronized with the phase of the transmitted pulse. The elements in a simple pulsed Doppler system are as follows: A CW sine and cosine reference signal are generated at the carrier frequency. A gate signal periodically directs one of the reference signals to the transmitter. The received echo is heterodyned by both reference signals, in two parallel multipliers. The outputs of the two multipliers are low-pass filtered, passing only the Doppler frequency resulting from scatterer motion. If the output of one channel is plotted as a function of the output of the other channel, the position of the point will rotate with time. The rate and sense of rotation give the magnitude and sign of the Doppler shift.

It is not difficult to implement the hardware for the tasks mentioned above. However, in practice it is useful to have control over the pulse length, repetition frequency, carrier frequency, as well as a number of other functions. This tends to complicate the design. Several years ago, a general purpose Doppler sonar controller was built at the Marine Physical Laboratory. It was designed to control and process up to eight different frequencies in parallel. The controller has been used with a variety of test transducers, as well as an 87.5 kHz array and a new 65-90 kHz 32 KW Doppler sonar. The design of the controller is discussed in this paper.

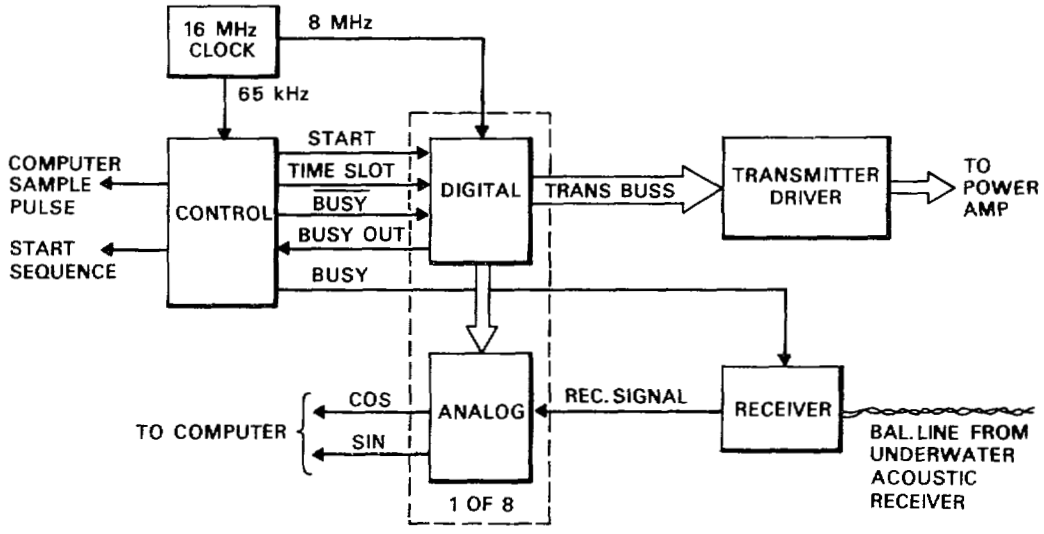

Figure 2. Sonar controller block diagram

System Description

The basic functions of timing, signal generation, heterodyning, etc., are accomplished in six different segments, each on a specific card. The cards are: first, a clock card which regulates system timing. Second, a controller card to generate all necessary timing functions. Third, a digital card that generates the transmitted frequency and determines when and how long the sonar will transmit at that frequency. Fourth, a transmitter card that isolates the digital cards from the sonars power amplifier. Fifth, a receiver card that converts the balanced line input to a single ended signal and buffers the output to the analog cards. Sixth, an analog or mixer card that does the heterodyning and filtering of the received signal.

This system requires one of each of the four control cards and one digital and analog card for each separate tone (Figure 2). The eight tone system, therefore, requires 20 cards. Each of the six types of card is discussed briefly below.

Oscillator Card

The oscillator card contains a 16.772216 mHz crystal oscillator that is used as a basic reference signal for the entire system. The 16 mHz is divided by 2 and is used by the synthesizer portion of the digital card. This clock is also divided by 256 to obtain the 65.536 kHz used by the control card. These outputs are buffered to isolate the clock from gate loading problems.

Master Control Card

Using the 65.536 kHz signal from the oscillator card the master control card generates four basic signals: The first is a master reset pulse. This pulse determines the repetition time of the eight tone sequence. This time can be varied from .94 seconds to 2.25 seconds in approximately .25 second steps. The second signal is a time slot pulse. There are 1024 equally spaced time slot pulses between each master reset pulse. The third signal is a sample pulse used by the computer to initiate the sampling of the received signal. This sample pulse rate can be adjusted from four pulses per time slot, to one pulse for each sixteen time slots depending on signal processing requirements. The fourth signal is the BUSY buss (active low). This signal is generated by anding the busy signals from each of the eight digital cards. The BUSY signal is then used by the digital cards to determine if it is permissible to transmit.

Digital Card

The digital card is the "smart" card in the system. This card determines when a tone is to be transmitted, how long to transmit, and at what frequency. These functions are accomplished in two separate sections; the control section and the frequency synthesizer (Figure 3).

The control section consists of two static registers and various logic circuits. The first register determines when to transmit, the second, how long. The registers are preset from switches

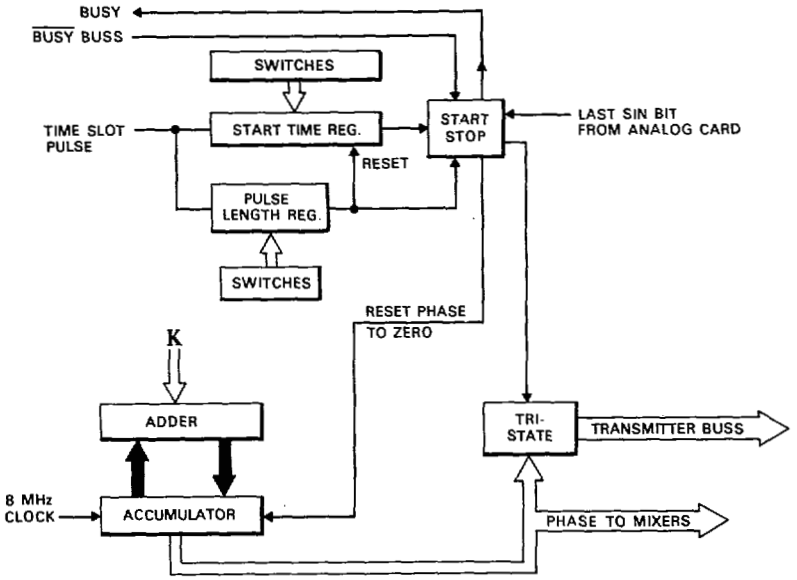

Figure 3. Digital card block diagram

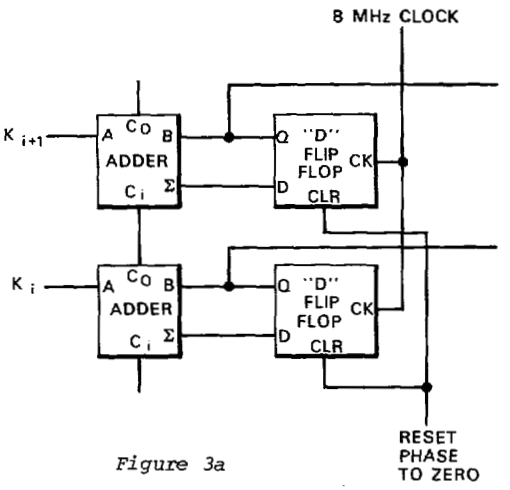

Figure 3a

Two typical stages of the phase accumulator

(with the compliment of the desired times). The master reset pulse loads the times into the registers. The "start register" then counts up with each time slot pulse. When the counter overflows the BUSY buss is checked to see if any other card is transmitting. If not, then the BUSY buss is pulled low by the control card to notify other cards that the transmitter is in use, the frequency synthesizer is reset so that the tone will start with a positive going zero crossing, and the tone duration register is enabled. If the BUSY buss is low (busy) then the digital card will wait for the buss to go high. As soon as the buss control goes high the digital card will then load the appropriate registers and start transmitting. This allows tones to be in adjacent time slots if desired. The time required to initiate transmission is small compared to the time slot duration.

The "tone duration register" counts up to a maximum of sixteen time slot pulses before it overflows, at which time it causes the start register to reset and the tone to be disabled. The "start register" will never overflow again before the next master reset pulse because it is a 12 bit counter (2048 counts) and there are only 1024 time periods. The BUSY buss is held low even after the tone is disabled. The transmission continues until the output of the frequency synthesizer reaches the next positive going zero crossing. At the zero crossing time the BUSY buss goes high and the transmission from this card ceases.

To keep large switching transients out of the power amplifier the transmitter is only turned on and off at zero crossings of the generated signal. This also means that all signals have an integer number of cycles. An additional consequence is that a tone is typically finished at a time later than the end of a time slot.

The digital frequency synthesizer (1,2) is used to generate the frequencies to be transmitted, as well as the continuous reference tone for the heterodyning circuit. Both the frequency and phase of the synthesized tone can be controlled. The synthesizer is composed of two major elements. The first is a phase accumulator register, which advances the phase of the waveform to be generated at a prescribed rate. The second element is a phase to amplitude converter, which associates an output voltage with each value of the phase. The phase to amplitude converter is not on the digital card, but rather on the analog signal processing card. Phase rate information is sent between these cards via a buss.

The phase accumulator consists of a 24 stage adder and a 24 stage storage register of "D" Flip Flops (Figure 3a). At each clock pulse, the storage register is incremented by a value K which is specified by a series of switches. The value in the accumulator is proportional to the phase of the waveform. The overflow rate of the accumulator is the frequency of the generated signal, F_o. The relationship of the output frequency to frequency control number, K , and clock frequency, F_c , is given by $F_o = KF_c/2^n$, where n is the number of bits in the register. With K restricted to integer values, frequency steps are in increments of $F_c/2^n$. In this synthesizer, $n = 24$ and $F_c = 2^{23}$. The frequency step size is, therefore, 1/2 Hz. The maximum frequency which can be generated depends on both F_c and the number of phase points at which the amplitude of the generated waveform is specified. In this controller, sine and cosine waves are generated. The values of sine and cosine amplitude are stored in PROMs at 32 discrete phase points. The highest frequency possible is generated when the phase is advanced $(2\pi)/32$

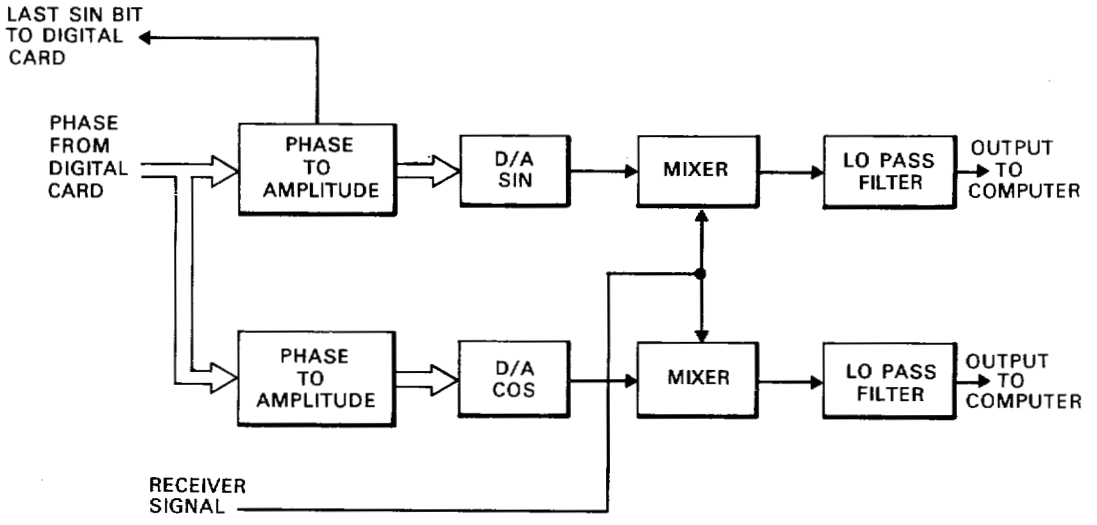

Figure 4. Analog card block diagram

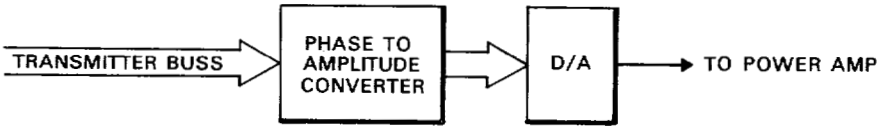

Figure 5. Transmitter card block diagram

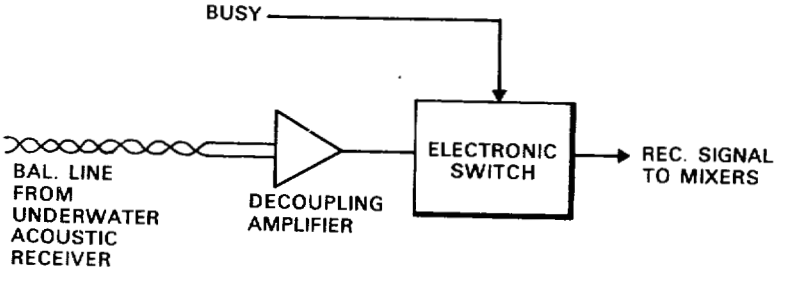

Figure 6. Receiver card block diagram

radians each clock pulse. This frequency is $F_{max} = F_c/32$, and is created for $K = K_{max} = 2^{19}$. The top five bits of the accumulator are used by the PROM to generate the digital amplitude information. These five bits are sent from the digital card to both the transmit card via a tri-state buss and to the analog card. The tri-state buss is enabled when the tone from a given digital card is to be transmitted.

It should be noted that this type of synthesizer does not advance the phase in time with perfect uniformity. The number of clock pulses required to overflow the phase accumulator can vary by one, depending on the value in the phase accumulator at the beginning of each overflow cycle. This phase jitter is associated with a spectral contribution near 32 F_o. This is not a significant problem for this application of the synthesizer. It can become significant if the output waveform is specified at a small number of phase points.

Analog Card

The analog card (Figure 4) has both a sine and a cosine PROM, the "phase to amplitude converter" portions of the frequency synthesizer, as well as a pair of mixer and low-pass filters. The output of each PROM is passed to a digital to analog converter and then to a current to voltage converter. In this manner, sine and cosine signals of considerable phase and amplitude stability are generated. These reference frequencies are fed into the carrier input of a balanced mixer. The other input of the mixer comes from the receiver amplifier. The mixer output is filtered by a 6 pole, three-section active filter. It has a break frequency of 50 Hz, and rolls off a 36 dB/octave down to -70 dB.

Transmitter Card

The transmitter card (Figure 5) uses the information on the tri-state buss and generates a sine wave during the transmit tone period. This is done by using a PROM, coded with a sine wave and D/A converter. This signal drives the sonars' power amplifiers.

Receiver Card

The receiver card (Figure 6) transforms the balanced signal that the hydrophone amplifier sends and converts it to a single ended signal. Because the receiver hydrophone is located very close to the transmitting hydrophones the receiver is overloaded during transmission. There is also some overload after the transmitter has stopped due to the high reverberation level close to the receiver. To help alleviate this problem an electronic switch is placed on the raw receiver output line that is controlled by the BUSY buss. This switch allows the output of the receiver amplifier to be turned off during the transmit time.

Conclusions

This controller has been used successfully with various Doppler sonars. The ability to precisely control tone duration, transmission time, and frequency has proven to be extremely useful. On the other hand, many binary numbers have to be manually switched into the various input registers to set up the system. This is a tedious task, in which errors are frequent. The only other source of awkwardness in this design is associated with the computer sample pulse frequency. This is linked to the time slot length and can only be adjusted by factors of two. It would be preferable to have a finer adjustment on the sample rate, and not have it linked to time slot duration. At sea, it is frequently difficult to change data recording computer programs by a factor of two in data rate.

A new controller is currently being designed to drive four sonars at sixteen different frequencies. The basic design of the new controller is similar to the one described in this paper. The major differences is that a microprocessor will do the control functions. This allows more versatility in choosing parameters of the different tones as well as ease in expanding the system.

Acknowledgements

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